We Claim:

1. An integrated memory, comprising:

command terminals for receiving command signals in a normal operation of the memory and in a test operation of the memory;

a signal terminal for receiving a further signal different from the command signals;

registers storing at least one of data patterns and data topologies used in the test operation of the memory; and

a register decoder circuit connected to said registers for selecting said registers, said register decoder circuit having inputs connected to said command terminals and to said signal terminal for selecting said registers in the test operation, said register decoder circuit selecting said registers in the test operation for reading out the at least one of data patterns and data topologies from said registers.

2. The integrated memory according to claim 1, further comprising:

a command decoder having inputs connected to said command terminals for receiving the command signals and connected to

the signal terminal for receiving the further signal, the further signal having a first state and a second state;

said command decoder generating a command for the test operation of the memory when the first state of the further signal is present at said signal terminal dependent upon the command signals;

said command decoder generating a command for the normal operation of the memory when the second state of the further signal present at said signal terminal depending upon the command signals; and

said register decoder circuit selecting a respective one of said registers associated with a respective command in the test operation.

3. The integrated memory according to claim 1, further comprising:

a command decoder having inputs connected to said command terminals for receiving the command signals and connected to the signal terminal for receiving the further signal, the further signal having a first state and a second state;

said command decoder generating a command for the test operation of the memory when the first state of the further signal is present at said signal terminal;

said command decoder generating a command for the normal operation of the memory when the second state of the further signal present at said signal terminal; and

said register decoder circuit selecting a respective one of said registers associated with a respective command in the test operation.

4. The integrated memory according to claim 2, wherein said signal terminal is connected to one of said inputs of said register decoder circuit and one of said inputs of said command decoder in a manner allowing changeover by a test mode signal.

5. The integrated memory according to claim 3, wherein said signal terminal is connected to one of said inputs of said register decoder circuit and one of said inputs of said command decoder in a manner allowing changeover by a test mode signal.

6. The integrated memory according to claim 2, wherein said signal terminal is connected to one of said inputs of said

register decoder circuit and one of said inputs of said command decoder and changes over between said one input of said register decoder circuit and said one input of said command decoder dependent upon a test mode signal.

7. The integrated memory according to claim 3, wherein said signal terminal is connected to one of said inputs of said register decoder circuit and one of said inputs of said command decoder and changes over between said one input of said register decoder circuit and said one input of said command decoder dependent upon a test mode signal.

8. The integrated memory according to claim 1, wherein said signal terminal receives a clock activation signal in the normal operation of the memory.

9. The integrated memory according to claim 1, wherein:

said command terminals are four command terminals;

said registers are four registers; and

said inputs of said register decoder circuit are connected said four command terminals and to said signal terminal for selecting said four registers in the test operation.

10. A method for testing an integrated memory, which comprises:

receiving command signals with command terminals in a normal operation of the memory and in a test operation of the memory;

receiving a further signal with a signal terminal, the further signal being different from the command signals;

storing at least one of data patterns and data topologies in a plurality of registers for use in the test operation of the memory;

connecting inputs of the register decoder circuit to the command terminals and to the signal terminal for selecting the registers in the test operation; and

selecting the registers with the register decoder circuit in the test operation and reading out the at least one of data patterns and data topologies from the registers.

11. The integrated memory according to claim 10, which further comprises:

connecting inputs of a command decoder:

to the command terminals for receiving the command signals; and

to the signal terminal;

generating a command with the command decoder for the test operation of the memory when a first state of the further signal is present at the signal terminal;

generating a command with the command decoder for the normal operation of the memory when a second state of the further signal present at the signal terminal;

selecting a register associated with a respective command with the register decoder circuit in the test operation.

12. The integrated memory according to claim 10, which further comprises:

connecting inputs of a command decoder:

to the command terminals for receiving the command signals; and

to the signal terminal;

generating a command with the command decoder for the test operation of the memory when a first state of the further signal is present at the signal terminal dependent upon the command signals;

generating a command with the command decoder for the normal operation of the memory when a second state of the further signal present at the signal terminal dependent upon the command signals;

selecting a register associated with a respective command with the register decoder circuit in the test operation.

13. The integrated memory according to claim 12, which further comprises connecting the signal terminal to one of the inputs of the register decoder circuit and to one of the inputs of the of the command decoder in a manner that allows changeover by a test mode signal.

14. The integrated memory according to claim 13, which further comprises connecting the signal terminal to one of the inputs of the register decoder circuit and to one of the inputs of the of the command decoder in a manner that allows changeover by a test mode signal.

15. The integrated memory according to claim 12, which further comprises changing over a connection of the signal terminal from one of the inputs of the register decoder circuit to one of the inputs of the of the command decoder dependent upon a test mode signal.

16. The integrated memory according to claim 13, which further comprises changing over a connection of the signal terminal from one of the inputs of the register decoder circuit to one of the inputs of the of the command decoder dependent upon a test mode signal.

17. The integrated memory according to claim 10, which further comprises receiving a clock activation signal with the signal terminal in a normal operation of the memory.

18. The integrated memory according to claim 10, which further comprises:

providing four command terminals and four registers; and

connecting the inputs of the register decoder circuit to the four command terminals and to the signal terminal for selecting the registers in the test operation.